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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,412	04/09/2004	Anders Landin	5681-01601	8427

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MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL, P.C.
P.O. BOX 398
AUSTIN, TX 78767-0398

EXAMINER	
ELAND, SHAWN	

ART UNIT	PAPER NUMBER
2188	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/821,412	LANDIN ET AL.	
	Examiner	Art Unit	
	Shawn Eland	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03/26/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Formal Matters

This Office action is in response to the Applicant's response filed on 03/26/07.

Status of Claims

Claims 1 – 38 are pending in the Application.

No claims have been amended.

There are no cancelled or new claims.

Claims 1 – 38 are rejected.

Response to Arguments

Applicant's arguments filed 03/26/07 regarding the address network have been fully considered but they are not persuasive. The memory and active device are part of element 32 in Liencres, which is connected to element 33.

Applicant's arguments, regarding sending a report and then sending the coherency message, see page 3, filed 03/26/07, with respect to the rejection(s) of claim(s) 1, 14, & 26 under Liencres have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of the combination of Liencres and Chandrasekaran.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 – 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Liencres*** (US 5,434,993) in view of ***Chandrasekaran*** (US 6,970,872).

In regards to claim 1, Liencres teaches a node ***(see element 20)*** including an active device ***(see element 21)***, an interface to an inter-node network ***(see element 31)***, a memory ***(see element 37)***, and an address network coupling the active device, the interface, and the memory **(see element 33)**; an additional node coupled to the node by the inter-node network ***(see figure 3a; see column 6, lines 11 – 15)***.

In regards to claim 14, Liencres teaches a plurality of devices including a memory ***(see element 37)***, an active device ***(see element 21)***, and an interface configured to send and receive coherency messages on an inter-node network coupling nodes in the multi-node computer system ***(see element 31)***; an address network configured to convey packets between the plurality of devices ***(see element 33)***.

In regards to claim 26, Liencres teaches an active device in the node initiating a transaction to gain an access right to a coherency unit by sending an address packet on an address network within the node ***(see element 21)***; an interface in the node ignoring the address packet ***(see element 35)***.

In regard to claims 1, 14, & 26, Liencres does not teach wherein in response to receiving from the active device an address packet initiating a transaction to gain an access right to a coherency unit, the memory is configured to send a report corresponding to the address packet to the interface if the transaction cannot be satisfied within the node. Liencres teaches ignoring the address packet ***(col. 7, lines 39 – 44)***, but does not teach in response to the report, the interface sending a coherency message to an additional interface in the additional node via the inter-node network, wherein the coherency message requests the access right to the coherency unit.

However, Chandrasekaran teaches a multi-node network ***(figure 1)*** that employs several techniques to reduce latency. One of the methods employed is "write-time" validity checking ***(col. 6, lines 25 – 36)***. When another node writes out data, it sends out a report stating the latest write time for that data. The read data is invalid once its timestamp comes before the latest write time. The node, now having an invalid read data, will ignore the current address packet ***(col. 2, lines 60 – 66)***, and then have to request the updated data from the additional node. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to employ optimistic reading of data using "write-time" validity checking so that reads could be employed when another node has exclusive access but hasn't yet written the data.

For claims 2, 15, & 27, Liencres teaches the node includes a data network coupling the active device, the interface, and the memory, and wherein the memory is configured to send the report to the interface in a data packet ***(see element 33)***.

For claims 3, 16, & 28, Liencres teaches the address packet is a read-to-own packet ***(see column 7, "Read Transactions")***, the access right is a write access right **(see column 2, lines 4 – 12; "owning" the data will give your write access)**, and wherein the memory is configured to

send the report corresponding to the read-to-own packet to the interface if a global access state of the coherency unit in the node is any global access state other than a modified global access state ***(see column 7, "Read Transactions")***.

For claims 4, 17, & 29, Liencres teaches wherein the node includes an additional active device ***(see element 35)***, wherein the additional active device is configured to transition a read access right to the coherency unit to an invalid access right upon receipt of the read-to-own packet ***(see column 7, "Read Transactions")***.

For claims 5 & 18, Liencres teaches the address network is configured to convey the read-to-own packet in broadcast mode, wherein the active device is configured to gain an ownership responsibility for the coherency unit upon receipt of the read-to-own packet ***(see column 4, lines 45 – 49)***.

For claim 30, Liencres teaches the address network conveying the read-to-own packet in broadcast mode; and the active device gaining an ownership responsibility for the coherency unit upon receipt of the read-to-own packet ***(see column 4, lines 45 - 49)***.

For claim 6, Liencres teaches an additional interface included in the additional node is configured to receive the coherency message on the inter-node network, wherein the additional interface is configured to send a proxy address packet on an address network included in the additional node in response to the coherency message ***(see column 7, "Read Transactions"; according to [00189] in the applicant's specification, proxy packets are packets sent by the interface 148; the processor cache controller 35 and the interface 148 are one and the same)***.

For claim 31, Liencres teaches an additional interface included in the additional node receiving the coherency message on the inter-node network; and the additional interface sending

a proxy address packet on an additional address network included in the additional node in response to the coherency message ***(see column 7, "Read Transactions"; according to [00189] in the applicant's specification, proxy packets are packets sent by the interface 148; the processor cache controller 35 and the interface 148 are one and the same)***.

For claims 7 & 19, Liencres teaches wherein in response to sending the coherency message, the interface is configured to receive an additional coherency message on the inter-node network; wherein in response to the additional coherency message, the interface is configured to send data corresponding to the coherency unit to the active device ***(see column 8, lines 56 – 62)***.

For claim 32, Liencres teaches the interface receiving an additional coherency message on the inter-node network, wherein the additional coherency message is responsive to the coherency message; in response to the additional coherency message, the interface sending data corresponding to the coherency unit to the active device ***(see column 8, lines 56 – 62)***.

For claims 8 & 20, Liencres teaches the active device is configured to gain the write access right to the coherency unit upon receipt of the data ***(see column 7, "Write Transaction")***.

For claim 33, Liencres teaches the active device gaining the write access right to the coherency unit upon receipt of the data ***(see column 7, "Write Transaction")***.

For claims 9 & 21, Liencres teaches the interface is further configured to send data corresponding to the coherency unit to the memory in response to the additional coherency message, wherein in response to the data, the memory is configured to update the global access state of the coherency unit in the node to the modified global access state ***(see column 7, "Read Transactions"; see column 1, lines 64 – 68 through column 2, lines 1 – 12)***.

For claim 34, Liencres teaches the interface sending data corresponding to the coherency unit to the memory in response to the additional coherency message; and in response to the data, the memory updating the global access state of the coherency unit in the node to the modified global access state ***(see column 7, "Read Transactions"; see column 1, lines 64 – 68 through column 2, lines 1 – 12)***.

For claims 10 & 22, Liencres teaches the memory is configured to send data corresponding to the coherency unit to the active device if the global access state is the modified state and if the memory has an ownership responsibility for the coherency unit, wherein the active device is configured to gain the write access right upon receipt of the data ***(see column 7, "Read Transactions")***.

For claim 35, Liencres teaches the memory sending data corresponding to the coherency unit to the active device if the global access state is the modified state and if the memory has an ownership responsibility for the coherency unit; and the active device gaining the write access right upon receipt of the data ***(see column 7, "Read Transactions")***.

For claims 11 & 23, Liencres teaches the address packet is a read-to-share packet ***(see figure 1a)***, the access right is a read access right ***(see column 7, "Read Transactions")***, and wherein the memory is configured to send the report corresponding to the read-to-share packet to the interface if a global access state of the coherency unit in the node is not a modified global access state or a shared global access state ***(see column 2, lines 15 – 29; the 2 nodes can share data as long as it is not modified)***.

For claim 36, Liencres teaches the address packet is a read-to-share packet ***(see figure 1a)***, the access right is a read access right ***(see column 7, "Read Transactions")***, and wherein

said sending the report occurs if a global access state of the coherency unit in the node is not a modified global access state or a shared global access state ***(see column 2, lines 15 – 29; the 2 nodes can share data as long as it is not modified)***.

For claims 12 & 24, Liencres teaches the interface is configured to add a record corresponding to the report to an outstanding transaction queue in response to receiving the report ***(see column 9, lines 32 – 47)***; wherein the interface is configured to add a record to the outstanding transaction queue in response to each address packet specifying a coherency unit that is not mapped by the memory ***(see element 40)***.

For claim 37, Liencres teaches the interface adding a record corresponding to the report to an outstanding transaction queue in response to receiving the report ***(see column 9, lines 32 – 47)***; and the interface adding a record to the outstanding transaction queue in response to each address packet specifying a coherency unit that is not mapped by the memory ***(see element 40)***.

For claims 13 & 25, Liencres teaches the interface is configured to send a corresponding coherency message on the inter-node network in response to each record in the outstanding transaction queue ***(see element 40; see column 9, lines 32 – 47)***.

For claim 38, Liencres teaches the interface sending a corresponding coherency message on the inter-node network in response to each record in the outstanding transaction queue ***(see element 40; see column 9, lines 32 – 47)***.

Conclusion

Khare (US 2002/0087811) teaches techniques for reducing latency in a multi-node network.

Examiner's Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Eland whose telephone number is (571) 270-1029. The examiner can normally be reached on MO - TH, & every other FR.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on (571) 272-4199. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Shawn Eland
06/22/2007

Kevin L. Ellis
Primary Examiner